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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/972,966	10/10/2001	John W. McCorkle	XSI.007	6238

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EXAMINER

LIU, SHUWANG

ART UNIT	PAPER NUMBER
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2634

DATE MAILED: 09/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/972,966	Applicant(s) MCCORKLE, JOHN W.	
	Examiner Shuwang Liu	Art Unit 2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 October 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 9-25 is/are rejected.
- 7) ☒ Claim(s) 1-8 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 10 October 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>10/14/03, 5/27/04</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Objections

1. Claims 1-8 are objected to because of the following informalities:
 - (1) In claim 1, line 1, insert - -Ultra Wide Bandwidth (UWB) - - after "A";
 - (2) In claims 2 and 4-8, line 1, insert - -UWB- - after "A", respectively;
 - (3) In claim 5, line 2, change "the" to - -an- -;
 - (4) In claim 9, line 3, change "UWB" to - - Ultra Wide Bandwidth (UWB)- -;
 - (5) In claim 11, line 2, change "UWB" to - - Ultra Wide Bandwidth (UWB)- -;
 - (6) In claim 15, line 2, change "UWB" to - - Ultra Wide Bandwidth (UWB)- -;
 - (7) In claim 19, line 2, change "UWB" to - - Ultra Wide Bandwidth (UWB)- -;
 - (8) In claim 20, line 13, change "UWB" to - - Ultra Wide Bandwidth (UWB)- -; and
 - (9) In claim 25, line 2, change "UWB" to - - Ultra Wide Bandwidth (UWB)- -.Appropriate correction is required.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section

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351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 10, 11, 14-16, 18-20, 22, 23 and 25 are rejected under 35 U.S.C. 102(e)

as being anticipated by Richards et al. (US 2002/0075976 A1).

As shown in figures 1B and 9, Richards et al. discloses:

(1) regarding claim 10:

a mode selection mechanism, comprising:

a clock signal generator (708) for generating a base clock signal at a base clock frequency (0097-0098);

a first divide circuit (912) for dividing the base clock signal by a first integer value M (2) to generate a first clock signal having a first clock frequency equal to the base clock frequency divided by M (0097-0098);

a second divide circuit (916) for dividing the base clock signal by a second integer value N (4) to generate a second clock signal having a second clock frequency equal to the base clock frequency divided by N (0097-0098); and

a switch (908) for selecting the first clock signal when a first receive mode of operation is selected, and for selecting the second clock signal when a second receive mode of operation is selected (0097-0098 and 0103).

(2) regarding claim 11:

wherein the first receive mode is a UWB receive mode (0014).

(3) regarding claims 14 and 18:

a mode selection mechanism in a multi-mode radio receiver, comprising:

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a mode selector (908) for selecting a receive mode of operation for a received signal,

an agile clock (708) for providing a base clock signal at a base clock frequency;

a frequency divider means (912 and 916) for dividing the frequency of the base clock frequency by an integer corresponding to the selected receive mode to generate a divided clock signal having a divided clock frequency (0097-0098 and 0103), and

a signal processor (136, 140 and 144) for processing the received signal with the divided clock signal.

(4) regarding claims 15 and 19:

wherein the selected receive mode of operation is a UWB mode (0014).

(5) regarding claim 16:

wherein the frequency divider further comprises:

a first frequency dividing unit (912), corresponding to a first receive mode, for dividing the frequency of the base clock frequency by a first integer to generate a first divided clock signal having a first divided clock frequency (0097-0098 and 0103), and

a second frequency dividing unit (916), corresponding to a second receive mode, for dividing the frequency of the base clock frequency by a second integer to generate a second divided clock signal having a second divided clock frequency (0097-0098 and 0103).

(6) regarding claim 20:

a multi-mode radio receiver, comprising:

a mode selection mechanism including

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an agile clock (708) for producing a base clock signal at a base clock frequency,
a first divide circuit (912) for dividing the base clock signal by a first integer to
generate a first divided clock signal at a first divided clock frequency,

a second divide circuit (916) for dividing the base clock signal by a second
integer to generate a second divided clock signal at a second divided clock frequency,
and

a switch (908) for providing a selected clock signal, the selected clock signal
being the first divided clock signal when a first receive mode of operation is selected,
and the second divided clock signal when a second receive mode of operation is
selected (0097-0098 and 0103); and

a UWB self-noise cancellation mechanism including
a pulse forming network (112, 120 and 132) for producing a series of UWB bi-
phase signals based on the selected clock signal,
a mixer (136) for combining the series of UWB bi-phase signals with an
incoming RF signal, and

an integrator (140) configured to accumulate an output of the mixer (0060).

(7) regarding claim 22:

wherein the first receive mode of operation is a UWB mode (0014).

(8) regarding claim 23:

a method of operating a multi-mode radio receiver, comprising:

generating a base clock signal (708) at a base clock frequency;

dividing the base clock signal by a first integer to generate a first divided clock

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signal at a first divided clock frequency (912) if a first receive mode is determined, and dividing the base clock signal by a second integer to generate a second divided clock signal at a second divided clock frequency (916) if a second receive mode is determined (0097-0098 and 0103).

(8) regarding claim 25:

wherein the first receive mode of operation is a UWB mode (0014).

3. Claims 10, 14, 16, 18, and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Sugasawa (US 6,249,445).

As shown in figures 12, Sugasawa discloses:

(1) regarding claim 10:

a mode selection mechanism, comprising:

a clock signal generator (CLK) for generating a base clock signal at a base clock frequency;

a first divide circuit (8) for dividing the base clock signal by a first integer value M to generate a first clock signal (CLK2) having a first clock frequency equal to the base clock frequency divided by M;

a second divide circuit (8) for dividing the base clock signal by a second integer value N to generate a second clock signal having a second clock frequency (CLK3) equal to the base clock frequency divided by N (0097-0098); and

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a switch (17) for selecting the first clock signal when a first receive mode of operation is selected (16), and for selecting the second clock signal when a second receive mode of operation is selected (column 12, line 66-column 13, line 62).

(2) regarding claims 14 and 18:

a mode selection mechanism in a multi-mode radio receiver, comprising:

a mode selector (16) for selecting a receive mode of operation for a received signal,

an agile clock (CLK) for providing a base clock signal at a base clock frequency;

a frequency divider means (8) for dividing the frequency of the base clock frequency by an integer corresponding to the selected receive mode to generate a divided clock signal having a divided clock frequency, and

a signal processor (1) for processing the received signal with the divided clock signal (column 12, line 66-column 13, line 62).

(3) regarding claim 16:

wherein the frequency divider further comprises:

a first frequency dividing unit (output CLK2 from 8), corresponding to a first receive mode (P2), for dividing the frequency of the base clock frequency by a first integer to generate a first divided clock signal having a first divided clock frequency, and

a second frequency dividing unit (output CLK3 from 8), corresponding to a second receive mode (P3), for dividing the frequency of the base clock frequency by a second integer to generate a second divided clock signal having a second divided clock frequency (column 12, line 66-column 13, line 62).

(4) regarding claim 23:

a method of operating a multi-mode radio receiver, comprising:

generating a base clock signal (CLK) at a base clock frequency;

dividing the base clock signal by a first integer to generate a first divided clock signal at a first divided clock frequency (output CLK2 from 8) if a first receive mode is determined, and dividing the base clock signal by a second integer to generate a second divided clock signal at a second divided clock frequency (output CLK3 from 8) if a second receive mode is determined (column 12, line 66-column 13, line 62).

4. Claim 9 is rejected under 35 U.S.C. 102(e) as being anticipated by McCorkle et al. (US 2003/0161411).

The applied reference has a common inventor with the instant application.

Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

As shown in figures 36 and 55, McCorkle et al. discloses a self-noise cancellation mechanism in a radio receiver, comprising:

means (242) for producing an internally-generated UWB bi-phase signal having a first arranged pattern;

means (200) for receiving an incoming RF signal having a second arranged pattern;

means (213-215) for combining the internally-generated UWB bi-phase signal and the incoming RF signal to produce an output; and

means (226-229) for integrating the output of the combining means over a length of time that corresponds with the first and second arranged patterns such that an integration output approaches zero when the incoming RF signal is aligned in phase with the internally-generated UWB bi-phase signal (0346) .

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 12, 13, 17, 21 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Richards et al. (US 2002/0075976).

Richards et al. discloses all of the subject matter except for teaching of that (1) the base clock frequency is about 4.8 GHz recited in claim 12 and (2) the second integer value N is equal to 2 as recited in claims 13, 17, 21 and 24.

Regarding claims although Richards et al. doesn't specifically disclose the limitations of (1) and (2) above, such limitation are merely a matter of design choice and

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would have been obvious in the system of Richards et al.. Richards et al. teaches that "In typical operation, the VCO clock may be 2.56 GHZ " (0101) and dividers can be used integers 2 and 4 for requirement of the designed system. The limitations in the claims do not define a patentably distinct invention over that in Richards et al. since both the invention as a whole and Richards et al. is directed to chose different integers for the divider and clock frequency for a typical operation. Therefore, to select different integer for divider and clock's frequency would have been a matter of obvious design choice to one of ordinary skill in the art.

Allowable Subject Matter

7. Claims 1-8 would be allowable if rewritten to overcome the objections, set forth in this Office action.

8. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to tech and suggest a self-noise cancellation comprising the first pattern and second pattern signals as recited in claim 1.

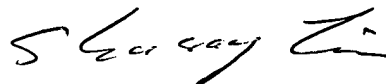
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shuwang Liu whose telephone number is 571 272-3036. The examiner can normally be reached on M-F, 7:30 AM to 5:00 PM.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 571 272-3056. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Shuwang Liu
Primary Examiner
Art Unit 2634

August 30, 2005